

Monolithic Integration of Quantum Resonant Tunneling Gate on a 22nm FD-SOI CMOS Process

Imran Bashir^{1,*,+}, Dirk Leipold^{1,+}, Elena Blokhina^{2,3,*,+}, Mike Asker^{1,+}, David Redmond², Ali Esmailian², Panagiotis Giounanlis², Hans Haenlein^{1,+}, Xutong Wu², Andrii Sokolov^{2,3}, Andrew K. Mitchell³, Dennis Andrade-Miceli^{2,3}, and Robert Bogdan Staszewski^{1,2}

¹Equal1.labs, Fremont, California, USA

²Equal1.labs, NovaUCD, Belfield, Dublin, Ireland

³University College Dublin, Belfield, Dublin, Ireland

*Corresponding Authors: imran.bashir@{equal1.com, ieee.org}, elena.blokhina@{equal1.com, ucd.ie},

ABSTRACT

The proliferation of quantum computing technologies has fueled the race to build a practical quantum computer. The spectrum of the innovation is wide and encompasses many aspects of this technology, such as the qubit, control and detection mechanism, cryogenic electronics, and system integration. A few of those emerging technologies are poised for successful monolithic integration of cryogenic electronics with the quantum structure where the qubits reside. In this work, we present a fully integrated Quantum Processor Unit in which the quantum core is co-located with control and detection circuits on the same die in a commercial 22-nm FD-SOI process from GlobalFoundries. The system described in this work comprises a two dimensional (2D) 240 qubits array integrated with 8 detectors and 32 injectors operating at 3 K and inside a two-stage Gifford-McMahon cryo-cooler. The power consumption of each detector and injector is 1 mW and 0.27 mW, respectively. The control sequence is programmed into an on-chip pattern generator that acts as a command and control block for all hardware in the Quantum Processor Unit. Using the aforementioned apparatus, we performed a quantum resonant tunneling experiment on two qubits inside the 2D qubit array. With supporting lab measurements, we demonstrate the feasibility of the proposed architecture in scaling-up the existing quantum core to thousands of qubits.

1 Introduction

Several quantum computing technologies are making inroads in the market today. The most commercially prevalent is the superconducting transmon qubit where a flux tunable critical current in a Josephson junction loop^{1,2} or superconducting quantum interference device (SQUID) controls the Pauli rotation about an axis on the Bloch sphere. The apparatus driving the transmon qubit is expansive (Fig. 1 in ref.³). In order to reduce the thermal excitation of the system, the transmon is placed in a dilution fridge operating at a base temperature of 10 mK. In this state, the flux-tunable transmon behaves like a quantum mechanical system where the driving signal amplitude or phase controls the XY rotation. The drive signal is generated by a rack mount arbitrary waveform generator (AWG) which is passed through mixers, attenuators, and couplers. The transmon qubit also includes a DC current port to tune the qubit resonance frequency and the current into that port is sourced by bias DACs. Lastly, the transmon qubit has a read-out port which is AC-coupled to a resonator. The qubit's state is determined by coupling an RF signal to the resonator and measuring the amplitude or phase shift of the reflected signal. The RF signal is coupled to the qubit through circulators and attenuators, while the reflected signal is amplified in multiple stages before being sourced to a measurement system. All the rack-mount control equipment such as AWGs, bias DACs, signal generators, and signal analyzers are located at room temperature whereas the couplers, mixers, attenuators, and circulators are strategically placed at multiple stages in the dilution fridge. Specialized coax cables for RF signals are used at each stage to minimize active and passive heating, especially at the base temperature stage where the thermal load of the dilution fridge (such as Bluefors XLD400 DR) is $19\mu\text{W}$ ⁴. This apparatus works reasonably well for small qubit counts (50-100) where the reported error rate is on the order of 0.1%⁵ and the qubit relaxation time (T_1) is $18.3\mu\text{s}$ ⁶. However, a fault-tolerant system requires a significantly large number of qubits which poses a challenge to the aforementioned approach when considering the amount of equipment, cabling, active and passive components required to facilitate control and read-out operation on such a quantum processor. Other challenges to scaling this technology to millions of qubits include frequency collision and crowding⁷.

On the other hand, semiconductor qubits offer a more efficient path to scaling⁸. In this technology, an electron's position or

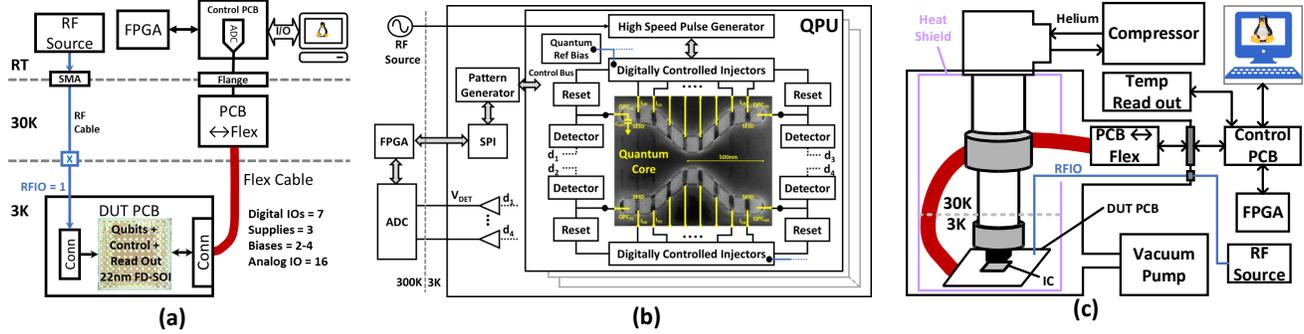


Figure 1. The quantum computer apparatus and top-level architecture. (a) Complete functional view of the quantum computer with cabling. The breakdown of the wiring on the flex cable is also shown. The 16 analog I/O wires are routed to the eight (8) on-chip detectors and can be eliminated with on-chip A/D. (b) Block level architecture of the Quantum Processor Unit. The 2D quantum structure, shown as (transmission electron microscopy) TEM micrograph, is co-located with control and read-out electronics on the same die. (c) Graphical representation of the Cryocooler apparatus and the interface between the IC and room temperature electronics.

spin is manipulated while they are confined in nanoscopic-scale quantum dots⁹. The number of qubits is scaled by placing a large number of quantum dots in an array. Pauli rotations are typically performed by driving a microwave signal and/or appropriate DC biasing to a control node to manipulate the electron's tunneling or spin blockade process while the qubits are placed in a dilution fridge with a base temperature of 20 mK. Read out can be done by sensing charge, current, or phase (for a gate-dispersive read out¹⁰). The key benefit of this approach is the advanced lithography process with which quantum dots with diameters as low as 45 nm¹¹ have been fabricated. However, the decoherence process of such qubits can be influenced by the nanoscopic charge fluctuation from the ²⁸Si/²⁸SiO₂ interface. That said, the qubits manufactured using this process have achieved a spin relaxation time (T_1) of 1.6 s, a spin dephasing time (T_2) of 24 μ s and single qubit gate fidelity of 99 %¹¹. Scaling the spin qubits count to millions will pose a challenge to route a large number of drive channels to the qubit array, especially when the control equipment resides at room temperature. The same will be true for detection channels if a gate-dispersive read-out method is used.

The obvious solution to cable management of a large number of wide-bandwidth I/O channels for qubit operation is to simplify the interface by deploying the control and detection hardware inside the cryocooler and closer to the qubit substrate. This complex integration task requires intimate knowledge of the cooling power and active and passive heat dissipation from circuits and cabling at each stage in the cryocooler. The first stage of the dilution fridge typically has a pulse tube cryocooler operating at 3 K with a thermal load specification of 1.5 W. This would be an ideal environment for a controller chip capable of driving a large number of excitation signals into a qubit processor while the number of wires to and from the room temperature electronics is reduced to a few control and trigger lines. Such controllers have been reported for transmon qubits⁶ and spin qubits^{12,13}. The same concept has been applied to cryogenic detectors for spin qubits using gate-dispersive read-out¹⁴ and transimpedance amplifiers¹⁵. In another published integration scenario, the qubit substrate and the controller IC is bonded to a common substrate at an elevated temperature stage of 100 mK¹⁶ while the driving circuits generating the excitation signal used a switch capacitor topology. The typical cooling power at this stage is 200 μ W, which is ten times higher than the 20 mK stage, however it is not large enough to accommodate meaningful integration with large number of channels. In another published work, the controller chip with single channel driver and detector was integrated with a double quantum dot structure on the same die¹⁷ operating at 110 mK. That solution cannot be scaled to a large qubit count due to the limited cooling power at the 110 mK stage.

This concludes the discussion on prior art and their unique characteristics. The benefits of the approach suggested in this paper and their distinction with the aforementioned references will be discussed in detail in the next section.

2 Key Innovation Factors

The architecture that will be described in this paper is unique from the prior art in several ways. Firstly, the cryogenic quantum control and read-out system is integrated with a two-dimensional (2D) qubit array in a single chip operating at 3 K as shown in Fig. 1(a). The result is a simplified and seamless interface between the cryogenic electronics and the qubit array. Only 30 wires are routed over a "flex" cable to the apparatus at room temperature. In addition to the flex cable, a single RF coax cable connects the IC to an external signal generator to receive the system clock. The digitization of the read-out signal is currently off-chip but can be straightforwardly relocated on-chip, reducing the wire count to the room temperature apparatus to just 14.

The thermal load of entire apparatus shown in Fig. 1(a) is 21 mW (see “Methods” section) which consumes only 1.5% of the 1.5 W cooling power at 3 K. The chip comprises an array of Quantum Processor Units (QPUs) as shown in Fig. 1(b). Each QPU houses a unique Quantum Core or the 2D qubit array. The qubit array is initialized by the reset transistors connected to the Quantum Point Contact (QPC) at the edges of the qubit array. This node is also shared with the detectors utilized during the read-out phase of the quantum experiment. The excitation signals for the qubits are sourced from digitally controlled injectors that are clocked by a high-speed pulse generator. The DC biasing of the qubit array is sourced from the Quantum Reference Bias Circuit (QRBC) coupled to the injectors¹⁸. Lastly, a pattern generator acts as a command and control block for all the aforementioned hardware interfacing the qubit array. The localized routing between the cryogenic electronics and the qubit array results in a power efficient control and detection system.

The second unique feature is the nature of the position-based charge qubit. The quantum dots in the qubit array shown in Fig. 1(b) are arranged over two rows in a “double-V” pattern¹⁹. In each row, the quantum dots are isolated by a barrier controlled by an imposer. The QPC acts as a reservoir from which a single electron is tunneled to the first quantum dot. The qubits are designed using “standard commercial” CMOS process without any application-specific tailoring of the layer stack or materials. This means that the thin film of Si above the oxide¹⁹ is not a pure isotope. Additional nanoscopic impurities will be present at the $^{28}\text{Si}/^{28}\text{SiO}_2$ interface. The quantum information is encoded in electron’s position controlled by a series of excitation signals applied at imposers to control the tunneling process of that electron across multiple quantum dots. The excitation signal can be a pulse²⁰ or resonant microwave signal²¹. In a pulse driven mode, the width of the pulse controls the evolution of electron’s wave function between the quantum dots while the DC biasing from the QRBC imposes a potential distribution across the wells²². In other words, the electron’s position or occupancy across quantum dots varies over the duration of the pulse at a rate known as Rabi Frequency. In the microwave driven mode, the excitation frequency must be resonant with Larmor frequency, which is determined by the difference between the ground and excited energy levels, while no DC magnetic field is applied to the qubit array. Once the quantum operation concludes, the read-out phase begins. During the read-out phase, the final state of the qubit is measured by sensing the charge present on the QPC node.

The third unique feature is the switched-capacitor topology of the cryogenic electronics. The signals driving the imposers in the qubit array can be synthesized with simple and power-efficient circuits labeled as injectors in Fig. 1(b). No active DC biasing is used in that block and the resulting transfer function is dependent primarily on the capacitors used in the design. Modeling of such circuitry can be done with reasonable accuracy as there is no dependency on transistor’s V_t or active currents which will vary significantly over temperature. The operating temperature is $100\times$ lower than room temperature and consequently the $\frac{kT}{C}$ is lower. Furthermore, the experimental data (see Sec. 4) proves that the charge can be stored on a capacitor for 100’s of μs due to the reduced leakage current at 3 K.

The fourth distinction is the system apparatus shown in Fig. 1(c). There is no bulky passive RF circuitry or magnets. The qubit array is designed in a flip-chip package and soldered onto the DUT PCB such that the backside of the die is flush with the cold finger at 3 K. The DUT PCB and flex cabling reside inside a heat shield with a penetration at the top for a two-stage Gifford-MacMahon (GM) cryocooler head. Helium-3 flows in the cryocooler through pipes connected between the compressor and the cryocooler head. The entire apparatus in Fig. 1(c), except for the compressor sits, inside a 6-ft server rack.

The aforementioned distinctions can also serve as headwinds in the qubit performance. The first and foremost is the elevated temperature of the qubit array as a direct consequence of the single-chip integration and the thermal load specification of the cryocooler. Moreover, without a pure ^{28}Si isotope, the decoherence process of this “hot” qubit array is influenced by the nanoscopic charge fluctuations caused by impurities. That said, characterizing the performance of charge and spin qubits under non-ideal conditions is an active area of research. Recently, Ramsey decay (T_2) of 75 ns and 200 ns was measured for a spin qubit at 3.5 K and 1 K respectively²³. Once performance trade-offs are understood and experimentally verified, the scientific community is likely to converge on a “sweet spot” temperature setting that addresses the challenges in scaling and integration with an acceptable qubit fidelity. The architecture presented in this paper is a practical demonstration of a reasonable compromise between these critical parameters. The reduced decoherence times, as a result of this compromise, also imply that the qubits must be ultrafast in terms of gate flip times. Such architectures are well suited for hybrid classical-quantum algorithms that operate on low-depth circuits.

Next, we will detail each block within the Quantum Processor Unit.

3 The Quantum Processor Unit (QPU)

3.1 Quantum Core

The quantum processor unit contains the 2D 240-qubit array and all control electronics in a $250\ \mu\text{m}\times 500\ \mu\text{m}$ cell as shown in the floor plan in Fig. 2(a). 32 injectors and 8 detectors surround the quantum structure. All circuitry is at a distance of $10\ \mu\text{m}$ from the quantum core. The area of the quantum structure is $4\ \mu\text{m}\times 2\ \mu\text{m}$, which is much smaller than the injector and detector circuits, and therefore, the wires from the quantum core have to fan-out to the surrounding circuits. The injectors comprise digital back-end and analog front-end circuitry. The analog front-end is an array of 16 capacitive DACs arranged in a tile²⁴.

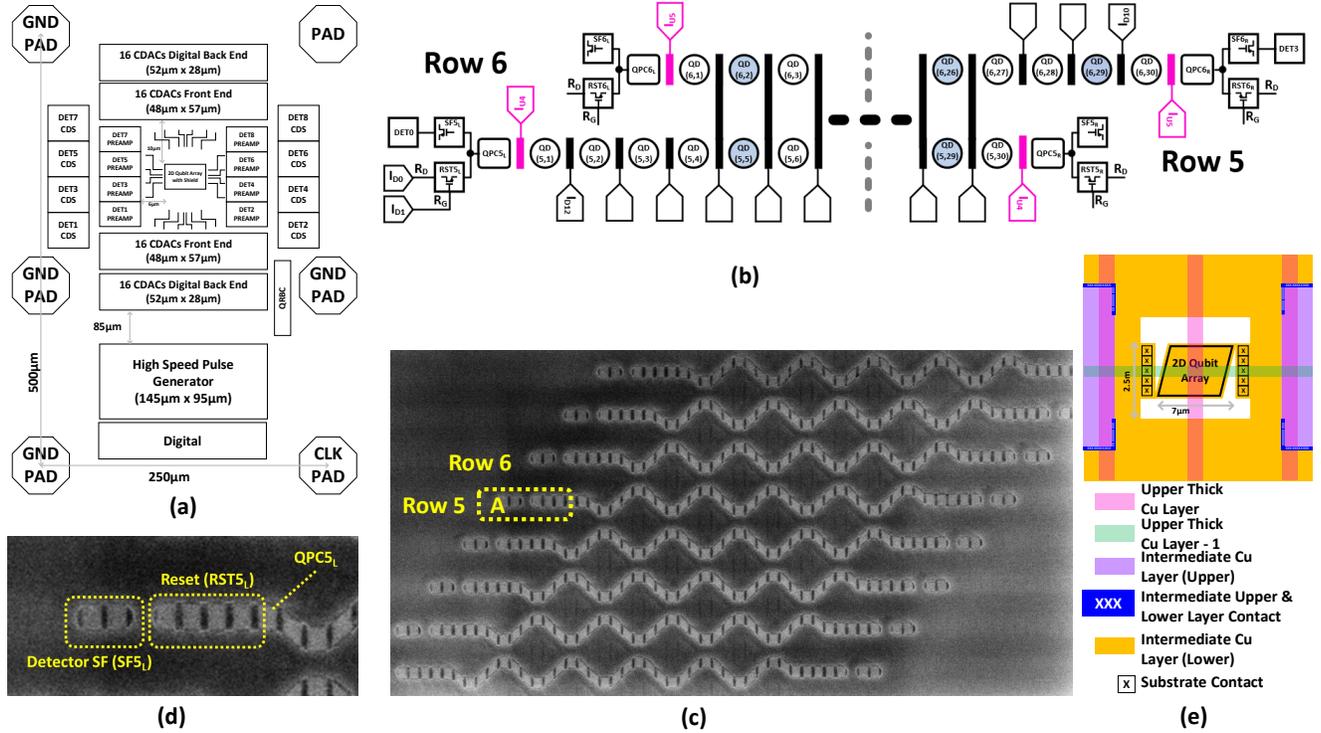


Figure 2. Details of Quantum Process Unit floor plan and the Quantum Core (a) Quantum Process Unit floor plan. The injectors are placed above and below while the detectors are placed on the left and right side of the 2D qubit array. (b) Detailed drawing of Rows 5 and 6 in the 240 qubit array spanning. The coupled quantum dots are colored blue. (c) TEM photograph of the 240 qubit array. (d) Zoomed version of region 'A' in (c) showing the detector source follower and the reset transistor. (e) Layout design of the heat shield around the quantum structure.

The DAC input code is stored in registers residing in the digital back-end along with custom synthesized logic. The clocks for these CDACs are sourced from the high-speed pulse generator, which is located in the lower half of the cell and next to a 2 GHz CLK pad. For the detector electronics, the CDS outputs are connected to a common row bus that is routed to the last stage of the detector chain. The map of the 240-qubit array and its TEM photograph is shown in Fig. 2(b) and (c), respectively. The 2D array is split into 8 rows and each row has 30 quantum dots. The notation of each quantum dot is $QD(x,y)$ where “x” and “y” indicate the row number (range 1–8) and the position (range 1–30). The solid line between the quantum dots indicates an imposer. The edge of each row terminates into a quantum point contact ($QPC_{X,L,R}$) and the imposer (colored pink) between the $QPC_{X,L,R}$ node and the first quantum dot is controlled by CDACs labeled I_{Ux} . The voltage from this CDAC controls the barrier and facilitates the transfer of a single electron from the QPC node to the first quantum dot. The remaining imposers control the tunneling of electron between neighboring quantum dots and perform Pauli rotations. The 8 rows in the 2D array are staggered, and when the line representing the imposer extends from one row to the next, it indicates that the imposers in those rows are controlled by a common CDAC. The sharing of CDACs is more frequent towards the middle of the array. The $QPC_{X,L,R}$ node is connected to reset and the source follower transistor as shown in the layout drawing in Fig. 2(d). Both of these devices are located close to the quantum structure in order to minimize the capacitance on QPC, which impacts the change in voltage as a result of single-electron transfer from this node. The reset transistor is a combination of four (4) stacked devices. A clearance of $10 \mu\text{m}$ is used around the quantum structure to facilitate routing which is done in low-level metal layers. Additional thermal insulation comes from a metal shield placed on an intermediate-level copper metal layer above the quantum structure. That layer is tied to the substrate with contacts around the 2D qubit array as shown in Fig. 2(e). The shield is tied to the straps running horizontally and vertically on the thick copper layers, which connect with three ground pads located near the quantum structure.

3.2 Quantum Reference Bias Generator

The quantum reference bias circuit is detailed in Fig. 3. The three critical nodes targeted for the dc biasing are the reset switch M_{RSTL} drain RD, gate RG, and imposer gates $I_{U/Dx}$ ($x = 1, 2, \dots$). Their respective baseline voltages are V_{RDPRE} , V_{RGPRE} , and V_{IPRE} . All these biases are sourced from a common reference V_{REF} that is external to the IC and has a long-term stability

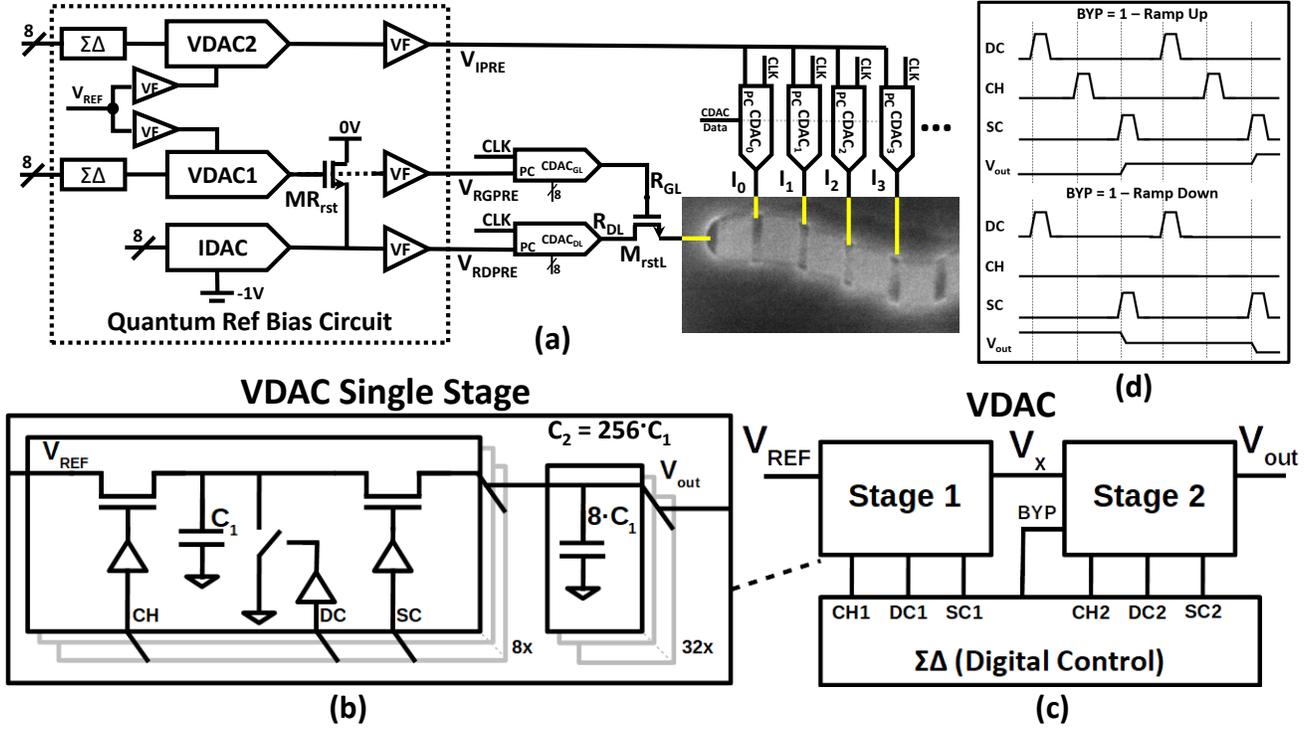


Figure 3. Quantum Reference Bias Circuit (QRBC). (a) Top level block diagram. (b) Single VDAC stage. The charge is redistributed between C_1 and C_2 . (c) Two cascaded VDAC stages. (d) VDAC signal sequence for output ramp up and down.

specification within ± 200 ppm. V_{REF} is located on the control PCB outside the cryocooler. Two voltage followers (VF) drive the reference input V_{REF} to the VDAC1 and VDAC2 blocks. The VDAC blocks are switched-capacitor arrays that redistribute the charge between C_1 and C_2 . Each VDAC comprises two cascaded stages for coarse and fine-tuning. The digital $\Sigma\Delta$ block generates pulses to discharge C_1 (DC), charge C_1 (CH), and transfer charge (SC) to C_2 based on an 8-b input. At the start, the DC, CH, and SC signals are pulsed in a sequence to ramp the output gradually towards the target. Once the output is around the target voltage, the CH pulse activity decreases. At this point, the resolution of the VDAC is approximately $300 \mu\text{V}$ given the capacitor ratio. Then, the second stage can be activated for finer adjustments to hit the target value. Next, the clock activity ceases, and the VDAC output is frozen before the CDAC pre-charge (PC) switch is enabled just before the quantum experiment commences. From this point onwards, any adjustment above or below the pre-charge level applied to the qubit array can be dynamically shifted by the CDACs based on their unique 8-bit digital control. V_{RDPRE} is generated by V_{gs} of a replica of the M_{pre} reset switch, MR_{pre} , and it is further adjusted by the 8-bit current DAC (IDAC) with a range from a few nA to $1 \mu\text{A}$ (max). In order to generate a negative V_{RDPRE} , IDAC V_{SS} is set to -1 V while MR_{pre} drain is at 0 V .

Two environmental factors work as tailwinds in this design. One is the reduced leakage current at cryogenic temperature (see Sec. 4). This implies that C_1 and C_2 can hold their charge long enough in cryogenic conditions for a quantum experiment to conclude, which typically takes 100's of ns. The other aiding factor is the lower kT/C noise at 3 K, which is 1/100th compared to the room temperature. Therefore, the capacitor size can be scaled down resulting in a miniaturized layout. The three internal voltage followers (VF) at the outputs shown in Fig. 3 are only needed when driving external pads for testing purposes and can be eliminated. All capacitors in the circuit are MOMCAPs designed with a stack of 3–5 intermediate metal layers. The circuits are designed with nominal V_{th} (RVT) transistors without any body biasing applied while the main supply is 0.8 V . The bias voltages applied to the quantum core have a maximum limit of $0.8 \text{ V} - V_{th}$ and a minimum limit of $-1 \text{ V} + V_{dsat}$, which is a sufficient range in order to conduct quantum experiments on the QDA. The typical clock frequency of the $\Sigma\Delta$ is 125 MHz and the switches in VDACS are sized appropriately to charge and discharge capacitor C_1 during the pulse duration of 8 ns . This gives reasonable dynamic power dissipation given the specified clock frequency. At the specified rate, VDAC outputs stabilize within $100 \mu\text{s}$ after activation.

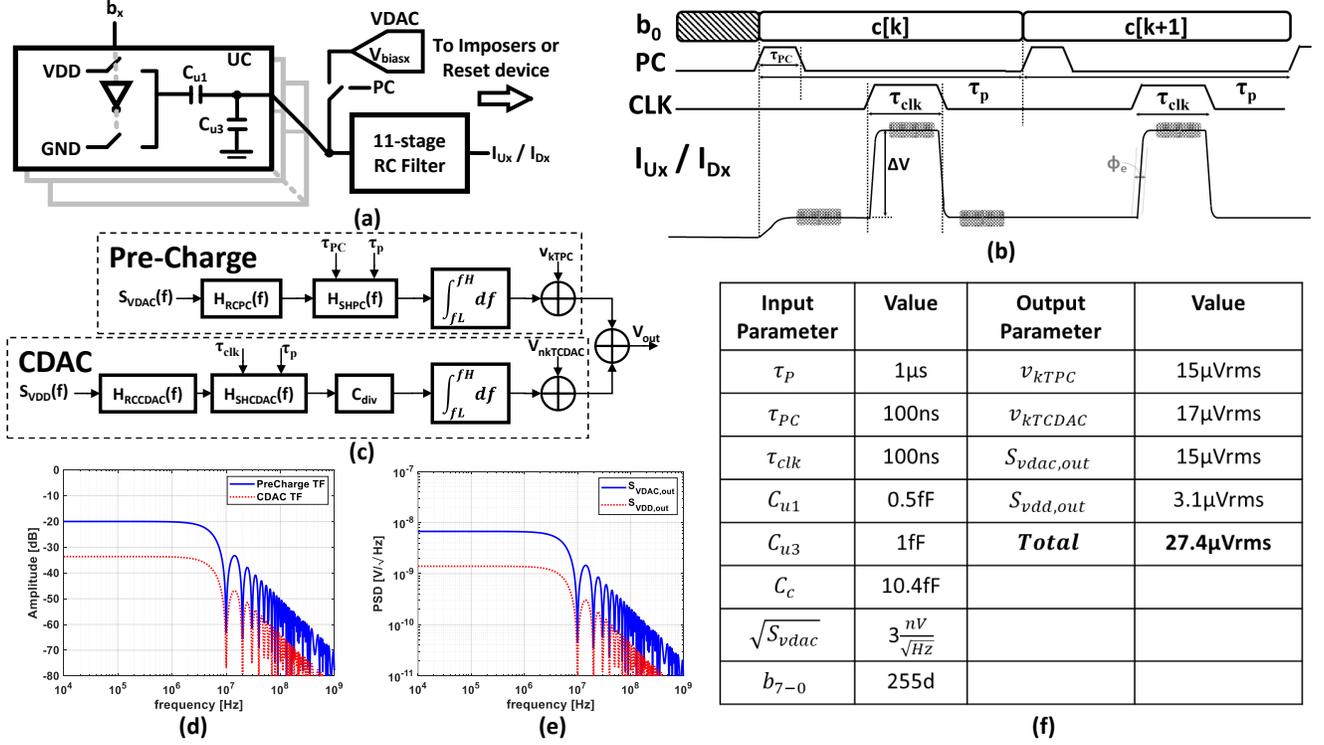


Figure 4. Injector functionality and noise characteristics (a) Block level diagram of the injector circuit. (b) Time-domain waveform of the injector output. The gray mesh region on the pedestal and step voltage represents noise. (c) Injector noise analysis with supply and VDAC noise at inputs. The noise is injected from the pre-charge and CDAC switch capacitor path and is summed together at the final output. (d) Amplitude response of transfer function of Pre-charge and CDAC path. (e) The VDAC and VDD noise spectra at the injector output. The noise from pre-charge path dominates the cumulative noise. (f) Noise model parameters and output noise summary.

3.3 Injector

The principal function of the injector²⁴ is to manipulate the reset device before and during the quantum experiment, control the barrier at the single-electron injection device, and to excite the imposers to control the evolution of electron's wave function in the intermediate quantum dots. The block diagram shown in Fig. 4(a) illustrates the injector function. First, the imposer node labeled I_{Ux} or I_{Dx} is pre-charged to a bias voltage V_{biasx} which is sourced from VDAC output inside the Quantum Reference Bias generator. This sets the pedestal of the voltage pulse shown in Fig. 4(b). Next, the digital code b_x activates the switch capacitor array, and a charge transfer takes place between C_{u1} and C_{u3} . This elevates the injector output by ΔV , which is digitally controlled. The 11-stage RC filter has a pole beyond 100 GHz and filters any ultra-fast transients on the imposer node.

The transfer function analysis shown in Fig. 4(c) considers the noise contribution from two paths: the pre-charge path and the switch capacitor array of the CDAC path. S_{VDD} and S_{VDAC} are the PSD of noise voltage on the V_{DD} supply and VDAC output, respectively. The transfer functions H_{RCPC} and H_{RCCDAC} model the RC filter formed by the switch resistance and output node capacitance. H_{SHPC} and H_{SHCDAC} model the aliasing of input noise due to the sample and hold operation²⁵ and is impacted by the timing parameters τ_p , τ_{PC} , and τ_{clk} . The formulas for these two transfer functions are derived in the "Methods" section. C_{div} is a scaling factor due to capacitive divider formed by C_{u1} and C_{u3} . The noise spectra in the pre-charge and CDAC paths are integrated over frequency and the resulting noise power is added to $\frac{kT}{C}$ noise (v_{kTPC} and v_{kTCDAC}) to compute the total noise at the injector output. Figure 4(d) compares the amplitude response in the "pre-charge" and the CDAC paths. The gain of the CDAC path is attenuated by C_{div} and, therefore, the VDAC noise at the injector output dominates the supply noise as shown in Fig. 4(e). Based on the circuit parameters defined in Fig. 4(f), the cumulative noise at the injector output is 27.4 μ V-rms.

3.4 Detector

The detector chain, shown in Fig. 5(a)²⁴, comprises the following stages: source follower, pre-amplifier, CDS (correlated double sampler), output buffer (OBUF), interface circuit with LPF, and ADC. The interface circuit and the ADC are off-chip components. The detector has to interface with a high-impedance node labeled QPC which is connected to the quantum

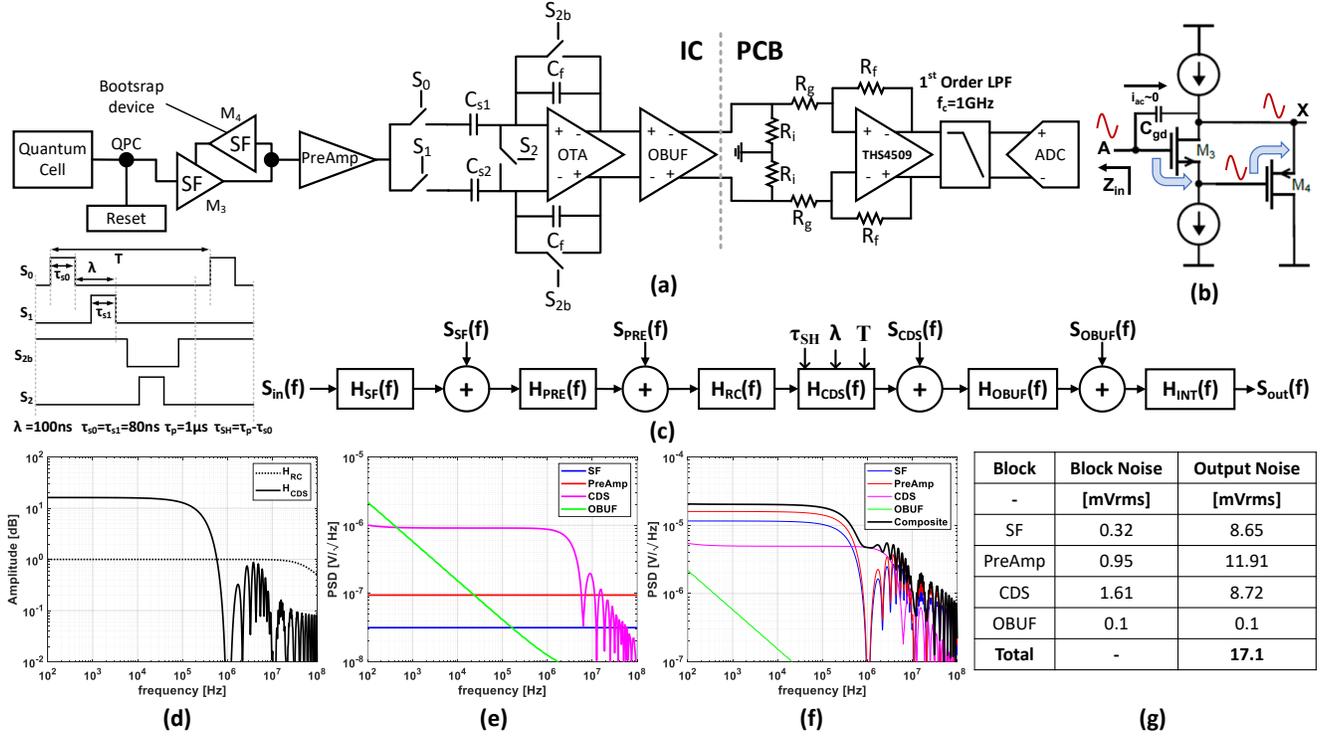


Figure 5. Detector chain noise sources and transfer function. (a) Block level diagram of detector chain. (b) C_{gd} neutralization using bootstrap device M4. (c) Frequency domain model of the detector chain. (d) H_{CDS} transfer function. (e) Spectra of noise sources used in the model. (f) Noise contribution from all sources at the detector output. (g) Summary of noise analysis.

structure and a reset device. A detector input impedance, which is substantially higher than the sourcing node (i.e. QPC) ensures a low loss transmission of the signal from the source node into the detector. For this reason, the source follower transistor M_3 in Fig. 5(b) is designed with minimum dimensions. However, any parasitic capacitance such as C_{gd} arising from M_3 can limit the input impedance of the detector. To address this issue, a bootstrapping device in the form of a source follower²⁶ M_4 is added to the circuit as shown in Fig. 5(b). This device creates a positive feedback at node A and forces the voltage at node A and X to move in tandem as a result of the perturbation caused by movement of charge from QPC during a quantum experiment. As a result, the current through C_{gd} and hence the impact of this capacitance is minimized.

Next, the transfer function of the detector chain will be analyzed. Figure 5(c) shows the transfer function from the QPC node till the ADC input. The source follower H_{SF} , the pre-amplifier H_{PRE} , and the output buffer H_{OBUF} transfer functions are assumed to be constant over frequency with a gain of 0.9, 2.2, and 5.4, respectively. H_{RC} is the RC response due to switch resistance and sample capacitor (C_{sx}) in the CDS, which has a pole around 70-MHz. H_{CDS} is the CDS transfer function which also accounts for aliasing of input noise due to the sample-and-hold operation and is impacted by three parameters shown in the timing diagram of Fig. 5(c): τ_{SH} , λ , and T . The derivation of this transfer function is based on^{25,27} and will be described in detailed in the “Methods” section. Figure 5(d) shows the H_{CDS} amplitude response with $\tau_{S0,S1}$, λ , and T set to 80 ns, 100 ns, and 1 μ s, respectively. H_{INT} models the ADC interface designed using a THS4509 op-amp and a low-pass filter. The resistor values for R_f and R_g are chosen such that the gain of the interface is 2. R_i sets the load line for the OBUF circuit, which is operating in class-A.

The spectra of noise sources in the detector are shown in Fig. 5(e). The pre-amplifier and the source follower noise is modeled as a white noise source in order to simplify the analysis of noise shaping due to H_{CDS} (see “Methods” section). The contribution of each noise source at the output is computed by multiplying the PSD of noise voltage by its respective transfer function. The results of that exercise are summarized in Fig. 5(f) and (g). The noise at close-in frequencies is dominated by the pre-amplifier and source follower due to the aliasing operation in H_{CDS} . The composite integrated noise at the detector output is 17 mV-rms, which is in line with the measurement reported in²⁴. It is important to note that the information from the quantum experiment that is stored in the capacitors C_{sx} is band-limited by the RC network modeled by H_{RC} .

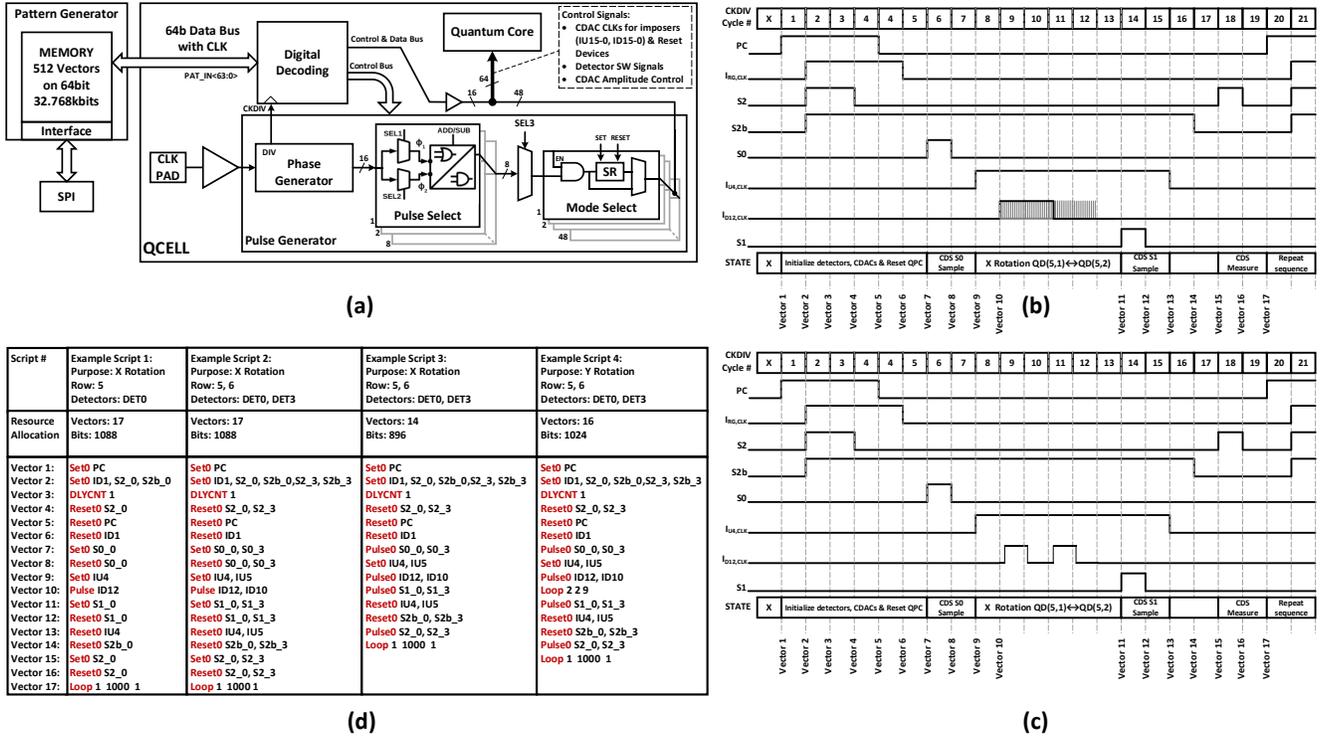


Figure 6. Pattern Generator, its data path, and four examples of resource allocation of pattern memory. (a) Data path flow from PATGEN output to the Quantum Core. The control signals from the pattern drive the Pulse Generator to synthesize precisely timed signals into the Quantum Core. (b) Signal timing of Example Script 1 in which an X Pauli rotation is performed using a pulsed excitation²⁰. (c) Signal timing of Example Script 4 in which an X Pauli rotation is performed using resonant driving²¹. (d) Summary table of four quantum experiment test scripts and their resource allocation.

3.5 Pattern Generator (PATGEN)

The pattern generator (PATGEN), shown in Fig. 6(a), acts as a command and control block in the Quantum Processor Unit and is integrated with the extensive electronics and the qubit array. The PATGEN comprises a memory core, an interface unit, and decoding logic. The interface unit handles the signaling between the 4-wire SPI and the PATGEN. The 32-kbit memory core has a depth of 512 while the data output bus is 64-bit wide. The memory core can store 512 vectors and a vector corresponds to a timing event caused by an instruction in the programming script. This will be explained in detail shortly. Inside the QCELL block, the 2 GHz clock is divided to generate CKDIV. The desired pattern is loaded into the memory core and channeled onto the 64-bit data bus while the timing of the pattern is based on CKDIV clock. The digital decoding block deciphers the incoming data and routes the information to two output ports: the control bus for the high-speed pulse generator²⁸ and the control and data bus for the Quantum Core. The 16 bit data bus for the quantum core contains the 8-bit CDAC amplitude word and some control signals. The remaining 48-bit control lines are clock signals for the 32 CDACs and control signals (CDS switches) for the eight (8) detectors. The clock and control signals are generated by the pulse generator and that process is described next.

The first stage of the pulse generator is a Phase Generator designed using a 16-stage Johnson counter that generates multiple signals with a phase separation of 500 ps for a 2 GHz clock. The clock frequency also sets the timing resolution of the pulse generator. Two signals from the Johnson counter are chosen for a programmable AND/OR operation, which either narrows or expands a pulse in the Pulse Select block. Up to 8 of these blocks run in parallel while each leaf cell has its unique set of SEL1, SEL2, and AND/OR selection codes in order to generate multiple signals with varying pulse-widths at the same time. This is a useful feature when there is a need to switch between two different timing profiles seamlessly. Finally, one output is selected to be passed to the Mode Select block which either propagates the input to the output or passes it to a SR (set/reset) latch. The latter option allows the pulse duration to be extended over longer time scales.

After describing the hardware implementation, it is important to discuss the programming and resource allocation per quantum operation or, more specifically, an X Pauli rotation. The nature of the Pauli rotation exhibited by the charge qubit is a function of energy levels and well potential over the qubit array in addition to the waveform applied to the imposer²⁹. The pattern shown in Fig. 6(b) and its corresponding program script in Fig. 6(d) (Example Script 1) is an example of a pulse-driven

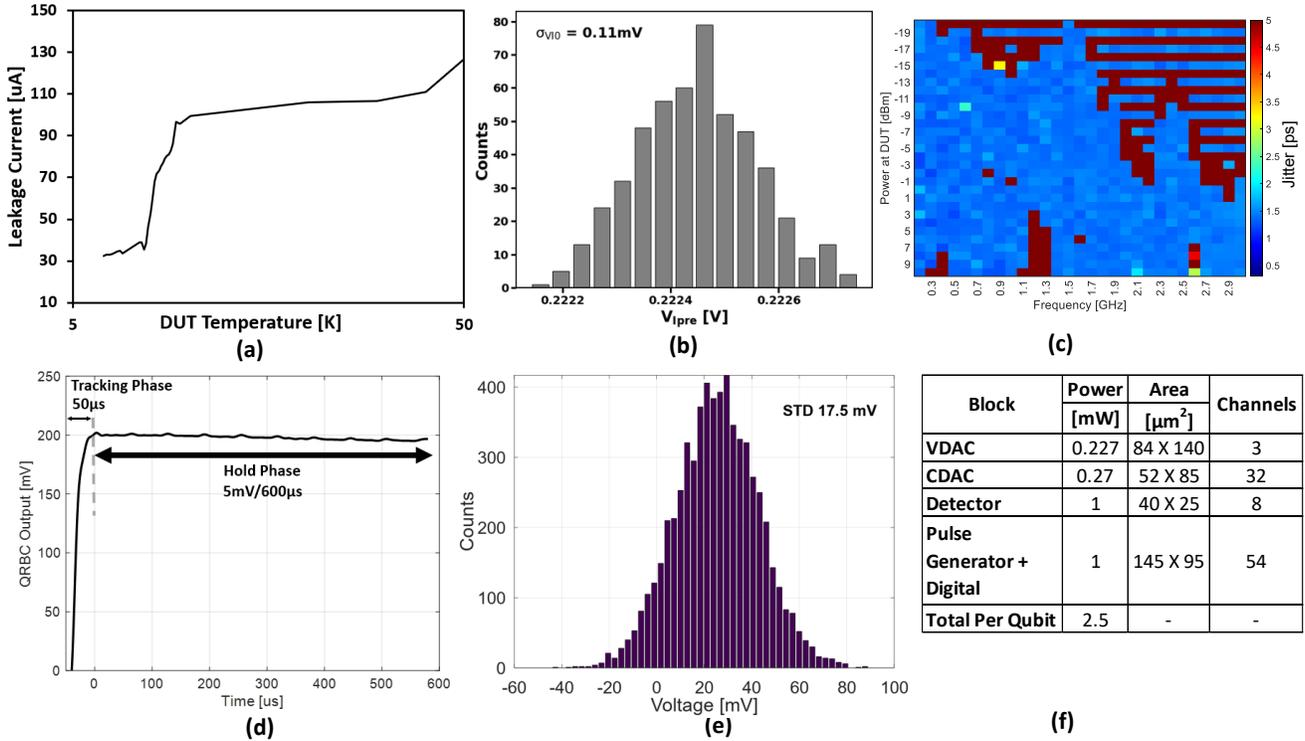


Figure 7. IC Measurements. (a) Total IC leakage current over temperature. (b) Noise at Quantum Reference Bias Circuit (QRBC) output connected to the imposer. (c) Heat map of RF clock jitter over signal generator frequency and power. (d) QRBC output over long time span. The output droop is negligible over $100 \mu\text{s}$ and 5 mV over $600 \mu\text{s}$. (e) Detector output noise measured at 3K . Standard deviation is 17.5 mV . (f) Summary of power of the entire control and detection circuits including the digital blocks such as the pulse generator and the PATGEN. The total power budget is 2.5 mW per qubit.

X rotation. This example has 17 vectors or instructions and each is annotated by a colored font. The number preceding the instruction links that instruction with the Pulse Select block number. For instance, the Set0 and Set1 commands are generated by Pulse Select Leaf Cell no. 1 and 2 out of the eight leaf cells. Pulse0 generates a rising and falling edge based on the 16 phases of the Johnson counter output. This is very useful in quantum experiments where fine timing resolution is required. The Loop command at Vector 17 allows the sequence to be repeated 1000 times (2nd parameter) while the 3rd parameter (1 in this case) indicates the Vector number to start the loop from. The total memory allocation for this script is 1088 bits ($17 \times 64\text{b}$) and the quantum operation is only isolated to quantum dots QD(5, 1) and QD(5, 2) in Row 5 of the qubit array (coupled to DET0) as shown in Fig. 2(b) and (c).

In the next step, the benefit of the parallel bus operation of the pattern generator is realized in Example Script 2 (Fig. 6(d) third column) where multiple node names are added to the same Vector. The same X rotation script now operates on four quantum dots over two rows and two detectors (DET0 and DET3); however, the memory utilization remains unchanged. Example Script 3 is a more area efficient rendering of the aforementioned script where the memory utilization is down to 896 bits. Example Script 4 in the last column column in Fig. 6(d) performs a X Rotation using a resonant driving method²¹ which is facilitated by the nested loops. The nested loop is at Vector 11 and loops two times starting from the position of Vector 9. This useful technique results in a memory allocation of 1024 bits, which is not too far from Example Script 3. In summary, the key feature in this design is a memory efficient instruction set operating on the pattern generator to create signals on the 64-bit bus which enables highly versatile operation on a large qubit array, such as the one presented in this work.

4 Measurement Results

The measurements presented in this section are divided into classical electronic measurements and quantum experiment measurements. Fig. 7 underscores the benefits arising from the low-temperature environment that acts as tailwind in cryogenic control circuit design. One of these is the low leakage current as demonstrated in Fig. 7(a) where the total leakage current of the entire IC goes down as the DUT temperature is reduced to 6 K . The low leakage allows the capacitor to hold its charge over a long period of time as shown in the time-domain quantum reference bias circuit (QRBC) output in Fig. 7(d). The QRBC

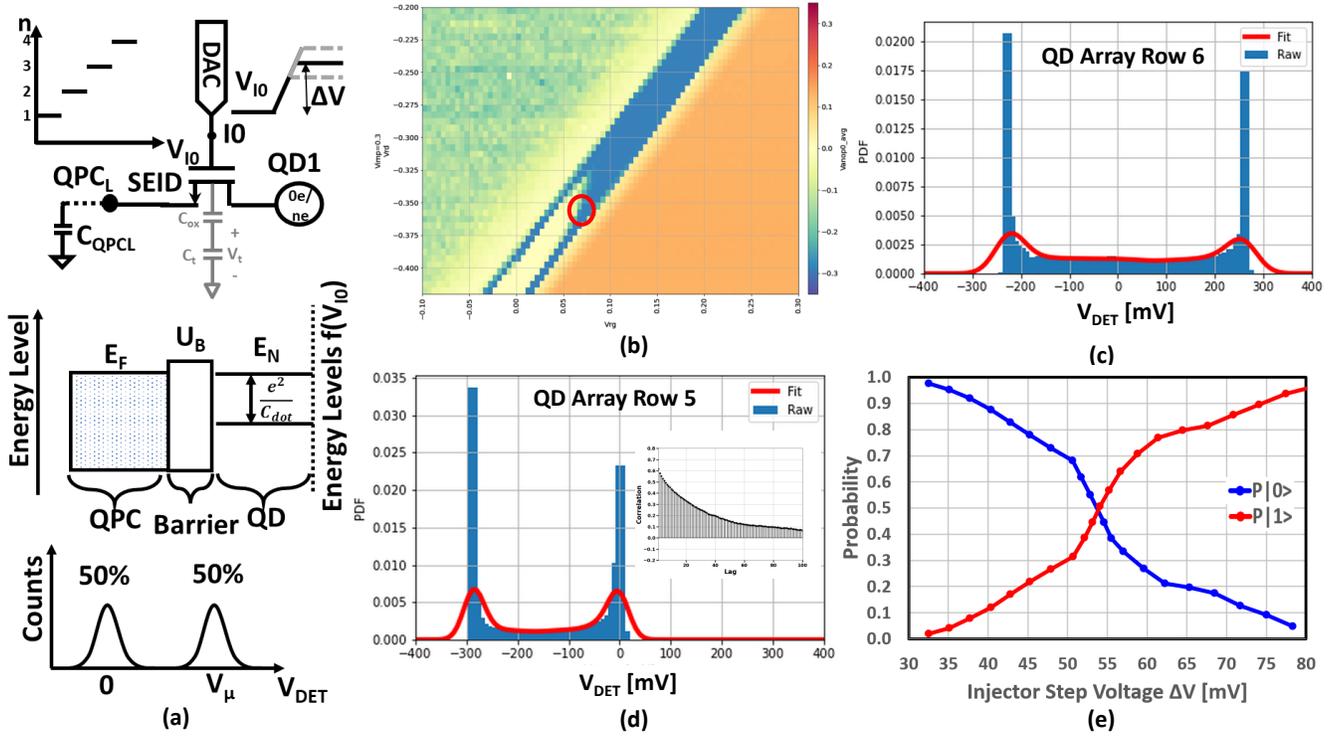


Figure 8. Experimental demonstration of Coulomb blockade at the SEID device on two rows of the 2D qubit array in Fig. 2(b). (a) Graphical representation of the condition required for quantum resonant tunneling. (b) Detector average voltage heat map as a function of reset transistor bias V_{RD} and V_{RG} . The region of interest is highlighted as the red circle where the detector output shows bi-modal signature. (c) The bi-modal detector output on DET3 located on 6th row in Fig. 2(b). (d) The bi-modal detector output on DET0 located on 5th row in Fig. 2(b). The figure inset shows the auto-correlation function and the response highlights a key characteristic of quantum resonant tunneling process^{31–33}. (e) $P|0\rangle$ and $P|1\rangle$ probability as a control function of injector step voltage similar to the gate modulation of probability in ref.^{31–33}.

output stabilizes in $50 \mu\text{s}$ and it remains so for nearly $100 \mu\text{s}$ during the hold phase. The long-term droop in the QRBC output is only 5 mV in $600 \mu\text{s}$. The QRBC output driving the imposer is measured over thousands of trials, and the output distribution is plotted in Fig. 7(b). The standard deviation of this distribution is $110 \mu\text{V}$ which is lower than the $\frac{kT}{q}$ limit of $267 \mu\text{V}$ at 3 K . Fig. 7(c) demonstrates the robustness of the high-speed pulse generator, which relies on an off-chip coax cable and frequency tuning elements³⁰. The clock signal path should be low loss over a wide bandwidth, which enhances the operating range and resolution of the pulse generator. Low level of mismatch implies that the DUT can operate at low output power from the signal generator, reducing the amount of active heat dissipation. The heatmap shown in Fig. 7(c) indicates a large range of frequencies and signal powers at the DUT input where the clock jitter is around 1.5 ps . This performance is achieved at the highest frequency of 2.5 GHz at -10 dBm delivered into the DUT. Fig. 7(e) is the detector noise measurement which is in line with the theoretical calculations detailed in Sec. 3.4. The total power consumption of all the blocks required to operate on one qubit is summarized in Fig. 7(f).

Fig. 8 details the quantum measurements performed on quantum dots located on rows 5 and 6 (coupled to DET0 and DET3) respectively of the 2D qubit array in Fig. 2(b). A sequence similar to the one shown in Fig. 6(b) is applied. The QPC node can be initialized by first scanning voltages on the reset transistor gate (R_G) and drain (R_D). The imposer connected to the single-electron injection device (SEID) is pulsed with a set amplitude during this scan. The detector output is stored over many iterations and the average value is plotted as a heat map in Fig. 8(b). In this plot, the region highlighted by the red circle is of particular interest where the detector output shows a bi-modal behavior. At this bias point, the conditions for quantum resonant tunneling depicted in Fig. 8(a) are met. The detector output distribution shows two distinct peaks when the barrier with potential energy U_B is low while the Fermi energy level E_f at QPC aligns with a discrete energy level in the adjacent quantum dot E_N . The outcome of each experiment is one of two possibilities. Either the electron tunnels to the adjacent quantum dot resulting in a loss of charge at QPC sensed by the detector resulting in a output voltage V_μ . The probability of this event is $P|1\rangle$. In the other event, the electron does not tunnel resulting in a detector output at 0 V . The probability of this event is $P|0\rangle$. Figures 8(c)

Parameter	This Work	JSSC'20 [10]	JSSC'19 [3]	Nat. Electronics [12]	ISSCC'20 [13]
Temperature	3K	3K	3K	100mK	110mK
Qubit Technology	Charge qubits	Spin qubits & Transmons	Transmons	-	Double Quantum Dot
Integration	Single Chip (3K): Quantum Core + Injectors + Detectors	Two chip: Quantum Processor (10-20mK) & Controller (3K), External readout		Two chip (100mK): Quantum Processor & Controller, Ext readout	Single Chip (110mK): Double Qdot + Single driver & Detector
Channels	32 injectors / 8 detectors	32 (128 with 4 TX)	1	32	1
Waveform Instructions	512 64-bit parallel vectors [†]	Upto 40960 pts AWG	Fixed 22 pts symmetric	128 bits	-
Instruction Set	Yes	Yes	No	-	-
Power	5mW / qubit (analog + digital + readout)	Analog: 1.7mW/qubit Digital: 330mW	Analog < 2mW/qubit	18nW per CLFG cell	0.295mW per QIC†
Chip Area	0.2mm ²	4mm ²	1.6mm ²	2.25mm ² ‡	0.01mm ²
Technology	GlobalFoundries Inc. 22nm FDSOI CMOS	Intel 22nm FinFET CMOS	28nm bulk CMOS	28nm FDSOI CMOS	28nm FDSOI CMOS

* Total instructions stored is limited to 512 however the rich instruction set and 64-bit parallel bus allows parallel & diverse operations on many qubits simultaneously.

‡ Published chip area is 6.25mm² however only the area of the FSM and CLFGs is accounted here.

† Includes power consumption of oscillator, single driver, and single TIA.

Figure 9. Comparison with prior art.

and (d) show the histograms of detectors DET3 and DET0 respectively when the reset transistor is biased properly and the events associated with the two states, namely $|0\rangle$ and $|1\rangle$, are clearly visible with a separation of 300 mV between them at the detector output. The quantum resonant tunneling process is moderately correlated when the lag is short as shown in Fig. 5 in ref.³¹. This unique characteristic is also observed by performing auto-correlation on the time series data of the detector samples and the result is shown in Fig. 8(d) inset. $P|1\rangle$ increases with increasing step amplitude of the SEID injector (or CDAC code) while $P|0\rangle$ retrogrades as shown in Fig. 8(e). This is yet another characteristic of quantum resonant tunneling also shown in Fig. 3 of ref.³¹ and Fig. 9 of ref.³². The x-axis in this chart has been translated from CDAC code a step voltage (based on Fig.8(a) in ref.²⁴). Therefore, we infer that in this state, the electron injection process is precisely controlled by a digitally controlled circuit parameter allowing us to manipulate the quantum information in two quantum dots (Row 5 and 6) in the 2D qubit array.

5 Conclusions

We have presented a monolithic integration of a quantum resonant tunneling gate with a quantum controller and read-out system. The entire apparatus operates on a low power budget of 2.5 mW per qubit. This figure of merit will improve further with on-chip digitization of detector output and reduce the cabling to room temperature electronics down to 13 wires. The monolithic integration is performed in “standard commercial” CMOS technology. The power efficient architecture of cryogenic electronics is enabled by switch capacitor implementation which is able to hold charge well over the time period required for a quantum experiment. The measurement results demonstrate a precise control of coulomb blockade and the electron injection process in two rows of the 240 qubit array. The total thermal load (calculated in “Methods” section) with current apparatus is 1.5% of the available cooling power at 3 K and still remains well below the 1.5 W limit when the 2D qubit array is scaled to 2400 qubits.

Methods

Experimental Data Processing

This section details important calculations associated with Fig. 8(c,d,e). The difference in V_{DET} between $|0\rangle$ and $|1\rangle$ of 300 mV can be translated to voltage fluctuation of 3.75 mV based on a simulated gain of the detector chain of 80 V/V²⁴. This is a factor of 12x higher than $\frac{kT}{q}$ limit of 300 μ V and gives us a reasonable SNR at the detector input. However, the fluctuation of the signal at the QPC node due to resonant tunneling process is wide-band and can't be processed by the detector. Consequently, there are counts appearing in the middle zone i.e. V_{DET} values between -290 mV and -10 mV in Fig. 8(c,d). Those events have been removed when analyzing probabilities shown in Fig. 8(e). The total counts for $P|0\rangle$ is determined by adding events in three bins in Fig. 8(c,d): -300 mV bin and two adjacent bins. Similar process is applied to compute total counts for $P|0\rangle$ around 0 mV bin. The probability is simply the ratio of the event counts and the total sample space (10k). The probabilities are plotted for a range of injector step voltages in Fig. 8(e).

Next, we estimate the difference in energy level ΔE which is given by $\frac{e^2}{C_{\text{dot}}}$ where e is the charge of an electron. In Fig. 8(e), $P|1\rangle$ fully transitions from 0% to 95% when the step voltage of the injector is increased from 33 mV to 78 mV. This 45 mV difference corresponds to a ΔV_t of 4.5 mV at the tunnel junction due to capacitive division from C_{ox} and C_t (see Fig. 8(a)). From this parameter, we calculate ΔE to be 4.5 meV and C_{dot} to be 35 aF. ΔE is 10x above the kT noise of 0.27meV at 3 K and C_{dot} value seems reasonable for a quantum dot of size 80 nm \times 80 nm.

Parameter	Value	Units	Parameter	Value	Units
Passive Load - Flex Cable			Active Load - Idd		
Thermal Conductivity ¹ (ρ_f)	250	[W/(m·K)]	Resistivity Cu (4K)	5.00E-10	[Ω·m]
Conductor Area (A_f)	6.56x10 ⁻¹⁰	[m ²]	Idd (Digital)	3.5	mA
Flex Cable Length (L_f)	0.393	[m]	Idd (Analog) ⁴	5.5	mA
Number of Wires ² (n_w)	35		P_{idd}	11.104	[mW]
P_{wire}	40	[uW]	Active Load - RF		
P_{flex}	1.4	[mW]	Cable Loss ³	2	dB
Passive Load - RF Coax Cable			P_{cable}	0.5	[mW]
Thermal Conductivity ³ (ρ_c)	122	[μW/(K)]	P_{term}	0.8	[mW]
Delta Temperature (ΔT)	60	K	P_{coax}	7.3	[mW]
P_{coax}	7.3	[mW]	Total Active Load	12.4	[mW]
Total Passive Load	8.7	[mW]	Radiative Load	0	[mW]
Total Thermal Load	21.1	[mW]	Cryocooler Limit (4K)	1.5	[W]

¹ Varies over temperature. See references.

² Five GND wires added to initial count of 30.

³ Based on data sheet of Lake Shore Cryotronics Type C RF Coax or measured data. See references.

⁴ Includes current from all eight detectors

Figure 10. Thermal load calculations. The calculations include active and passive loads from cabling connected to DUT including the RF coax carrying the chip clock. Some parameters in the table are taken from^{30,34}.

Heat Load Calculations

The heat load calculations, shown in Fig. 5, include active and passive loads due to cabling between the DUT PCB and the room-temperature electronics. Radiative loads are neglected in this analysis. The passive loads are calculated for 35 wires (30 from Fig. 1(a) plus five ground wires) on the flex cable and one RF coax wire. The thermal conductivity of copper $\rho_f(T)$ varies significantly from 3K to 60K³⁴ and therefore, the analysis calculates the area under the curve over that temperature range to compute the heat transfer due to the flex cable. The equation for the passive thermal load is⁴:

$$P_p = n_w \int_{3K}^{60K} dT \cdot \frac{\rho_f(T) \cdot A_f}{L_f} + \rho_c \cdot \Delta T \quad (1)$$

where A_f and L_f is the cross-section area and length of the conductor on the flex cable respectively, and n_w is the number of wires. The RF coax cable is the Lake Shore Cryotronics Type C cable³⁵ and its thermal conductivity ρ_c is defined in different units than ρ_f . The heat transfer from the RF coax is calculated by multiplying by the temperature difference between the cryocooler stages with ρ_c . For active load, the square of the average supply current is multiplied by the calculated wire resistance. The heat dissipation from the RF signal is due to the cable loss of 2 dB³⁰ and the 50 Ω termination at the 3K stage. The total thermal load is 21 mW which is 1.5% of the 1.5 W specification. If the 2D qubit array is scaled by a factor of 10 resulting in a 2400 qubit array, the number of detectors will scale to 160. The total thermal load (passive and active) in this case is 150 mW which is still well below the cryocooler specification. Moreover, on-chip digitization of the detector data will reduce the cabling and consequently the thermal load significantly.

Transfer Function for Noise Analysis at the Injector Output

The transfer function H_{SHPC} in Fig. 4(c) aliases the noise at the switch input and the extent of aliasing is controlled by the duration of pre-charge operation τ_{PC} and the cycle rate τ_p . This equation for H_{SHPC} is determined by modeling the track and hold operation exclusively and assuming the input noise is white over a finite bandwidth²⁵. During track mode, when the sample switch is closed, the output noise tracks the input. This time duration for this mode, τ_{PC} , is normalized to the switching period:

$$\tau_{PCn} = \frac{\tau_{PC}}{\tau_p}; \quad \tau_{SHn,PC} = 1 - \tau_{PCn}; \quad f_s = \frac{1}{\tau_p} \quad (2)$$

where $\tau_{SHn,PC}$ is the normalized hold period when the pre-charge switch is open. The input noise from the VDAC is assumed to be white with density S_{VDAC} over a bandwidth BW_n of 500 MHz used in this analysis. The equation for the transfer function

has the same form as Eq.6 in ref.²⁵:

$$H_{SHPC}(f) = 2\tau_{SHn,PC}^2 \left(\frac{BW_n}{f_s} \right) \text{sinc}^2 \left(\frac{\tau_{SHn,PC} f}{f_s} \right) + (1 - \tau_{SHn,PC}) \quad (3)$$

Similarly, the transfer function H_{SHCDAC} models the aliasing of the digital supply noise S_{VDD} to the injector output.

$$H_{SHCDAC}(f) = 2\tau_{SHn,clk}^2 \left(\frac{BW_n}{f_s} \right) \text{sinc}^2 \left(\frac{\tau_{SHn,clk} f}{f_s} \right) + (1 - \tau_{SHn}) \quad (4)$$

where $\tau_{SHn,clk}$ is the normalized hold period ($\tau_{clk}=0$) for the CDAC path in Fig. 4(c).

Detector CDS Transfer Function

The CDS transfer function in the detector shown in Fig. 5(c) can be analyzed from Eq. 5 in ref.²⁷.

$$H_{CDS}(f) = 4\text{sinc}^2(\pi f T) \cdot \sum_{n=-\infty}^{\infty} S_{in}(f - n/T) \sin^2[\pi\lambda(f - n/T)] \quad (5)$$

The “sinc” term in Eq. 5 is due to the sample and hold operation similar to ref.²⁵. The summation term of the input spectrum is the aliasing function. This analysis can be simplified if the input noise spectrum is assumed to be white over the band of interest which is 100 MHz in the numerical model. With that assumption, the summation term in Eq. 5 can be reduced to an analytical expression based on Eq. 3. The replacement term is $2\frac{BW_n}{f_s}$ which essentially is the number of sidebands that are aliased into the bandwidth of interest (see Eq.2 in ref.²⁵). A simple approach is to structure Eq. 5 as Eq.6 in ref.²⁵ and add the $\sin^2[\pi\lambda(f - n/T)]$ to account for the difference in two discrete Fourier transforms. Using this approach and the timing parameters shown in Fig. 5(c), the CDS transfer function is plotted in Fig. 5(d).

References

1. Knight, W. *IBM Raises the Bar With a 50-Qubit Quantum Computer*. <https://www.technologyreview.com/s/609451/ibm-raises-the-bar-with-a-50-qubit-quantum-computer> (2017).
2. Kelley, J. *A Preview of Bristlecone, Google's New Quantum Processor*. <https://ai.googleblog.com/2018/03/apreview-of-bristlecone-googles-new.html> (2017).
3. Staszewski, B., Bashir, I., Blokhina, E. & Leipold, D. Cryo-CMOS for Quantum System On-Chip Integration. *Solid-State Circuits Mag.* **13**, 46–53 (2021).
4. Krinner, S. *et al.* Engineering cryogenic setups for 100-qubit scale superconducting circuit systems. *Arxiv: 1806.07862v1* (2018).
5. Barends, R. *et al.* Superconducting quantum circuits at the surface code threshold for fault tolerance. *Nat. communications* **9**, 1–6 (2018).
6. Bardin, J. C. *et al.* Design and Characterization of a 20-nm Bulk-CMOS Cryogenic Quantum Controller. *Solid-State Circuits* **54**, 3043–3060 (2019).
7. Brink, M. *et al.* Device challenges for near term superconducting quantum processors: frequency collisions. In *IEDM*, 6.1.1–3 (2018).
8. Nikandish, R., Blokhina, E., Leipold, D. & Staszewski, R. B. Semiconductor quantum computing: Toward a cmos quantum computer on chip. *IEEE Nanotechnol. Mag.* 2–14, DOI: [10.1109/MNANO.2021.3113216](https://doi.org/10.1109/MNANO.2021.3113216) (2021).
9. Maurand, R. *et al.* A CMOS silicon spin qubit. *Nat. communications* **7**, 13575 (2016).
10. Crippa, A., Ezzouchm, R., Aprá, A. *et al.* Gate-reflectometry dispersive readout and coherent control of a spin qubit in silicon. *Nat. communications* **10**, 1–6 (2019).
11. Zwerver, A. M. J. *et al.* Qubits made by advanced semiconductor manufacturing. *Arxiv: 2101.12650v* (2021).
12. Van Dijk, J. P. *et al.* A Scalable Cryo-CMOS Controller for the Wideband Frequency-Multiplexed Control of Spin Qubits and Transmons. *Solid-State Circuits* **55**, 2930–2946 (2020).

13. Bonen, S. *et al.* Cryogenic characterization of 22-nm fdsoi cmos technology for quantum computing ics. *IEEE Electron Device Lett.* **40**, 127–130 (2018).
14. Ruffino, A., Peng, Y. *et al.* A fully-integrated 40-nm 5-6.5 GHz cryo-CMOS system-on-chip with IQ receiver and frequency synthesizer for scalable multiplexed readout of quantum dots. In *2021 IEEE International Solid-State Circuits Conference (ISSCC)*, 210–212 (IEEE, 2021).
15. Gong, M. J. *et al.* Design considerations for spin readout amplifiers in monolithically integrated semiconductor quantum processors. In *2019 IEEE Radio Frequency Integrated Circuits Symposium (RFIC)*, 111–114 (2019).
16. Pauka, S. J. *et al.* A cryogenic CMOS chip for generating control signals for multiple qubits. *Nat. electronics* **4**, 64–70 (2021).
17. Guevel, L. L. *et al.* A 110mK 295 μ W 28nm FDSOI CMOS quantum integrated circuit with a 2.8GHz excitation and nA current sensing of an on-chip double quantum dot. In *ISSCC, ses. 19.2*, 306–308 (2020).
18. Bashir, I. *et al.* Bias generation and calibration of cmos charge qubits at 3.5 kelvin in 22-nm fdsoi. In *ESSCIRC 2021 - IEEE 47th European Solid State Circuits Conference (ESSCIRC)*, 47–50, DOI: [10.1109/ESSCIRC53450.2021.9567784](https://doi.org/10.1109/ESSCIRC53450.2021.9567784) (2021).
19. Bashir, I. *et al.* A single-electron injection device for CMOS charge qubits implemented in 22-nm FD-SOI. *IEEE Solid-State Circuits Lett.* **3**, 206–209 (2020).
20. Gorman, J., Hasko, D. & Williams, D. Charge-qubit operation of an isolated double quantum dot. *Phys. review letters* **95**, 090502 (2005).
21. Dohun, K., Ward, D. R., Simmons, C. B. *et al.* Microwave driven coherent operations of a semiconductor quantum dot charge qubit. *Arxiv: 1407.7607v1* (2015).
22. Blokhina, E. *et al.* CMOS position-based charge qubits: Theoretical analysis of control and entanglement. *IEEE Access* **8** (2020).
23. Camenzind, L. C., Geyer, S., Fuhrer, A., Warburton, R. J. *et al.* A spin qubit in a fin field-effect transistor. *Arxiv: 2103.07369v1* (2021).
24. Esmailiyan, A. *et al.* A Fully Integrated DAC for CMOS Position-Based Charge Qubits with Single-Electron Detector Loopback Testing. *IEEE Solid-State Circuits Lett.* **3**, 354–357 (2020).
25. Fischer, J. H. Noise Sources and Calculation Techniques for Switched Capacitor Filters. *IEEE J. Solid State Circuits* **SC-17**, 742–752 (1982).
26. Chi, M. Y., Christoph, M. & Cauwenberghs, G. Ultra-High Input Impedance, Low Noise Integrated Amplifier for Noncontact Biopotential Sensing. *Emerg. Sel. Top. Circuits Syst.* **1**, 526–535 (2011).
27. Pimbley, J. M. & Michon, G. J. The output power spectrum produced by Correlated-Double Sampling. *IEEE Transactions Circuits Syst.* **38**, 1086–1090 (1991).
28. Bashir, I. *et al.* A mixed-signal control core for a fully integrated semiconductor quantum computer system-on-chip. In *Proc. of IEEE European Solid-State Circuits Conf. (ESSCIRC), ses. A2L-C4*, 1–4 (IEEE, 2019).
29. Giounanlis, P. *et al.* CMOS charge qubits and qudits: entanglement entropy and mutual information as an optimization method to construct CNOT and SWAP gates. *Semicond. Sci. Technol.* (2021).
30. Bashir, I. *et al.* RF Clock Distribution System for a Scalable Quantum Processor in 22-nm FDSOI Operating at 3.8K Cryogenic Temperature. In *2020 IEEE Radio Frequency Integrated Circuits (RFIC) Symposium. Digest of Papers, Los Angeles, CA, USA, 2020, pp. 215–218.* (IEEE, 2020).
31. Li, Z., Sotto, M., Liu, F. *et al.* Random telegraph noise from resonant tunnelling at low temperatures. *Sci. Reports* **8**, 1–9 (2018).
32. Li, Z. *et al.* Random-telegraph-noise by resonant tunnelling at low temperatures. In *IEDM*, 172–174 (2017).
33. Miki, H. *et al.* Statistical measurement of random telegraph noise and its impact in scaled-down high-K metal-gate MOSFETs. In *IEDM*, 19.1.1–19.1.4 (2012).
34. NIST. *Material Properties: OFHC Copper (UNS C10100/C10200)*. https://trc.nist.gov/cryogenics/materials/OFHC%20Copper/OFHC_Copper_rev1.htm (2010).
35. Shore, L. *Lake Shore Cryotronics Ultra-manifure cryogenic Coaxial Type C Cable*. <https://www.lakeshore.com/products/categories/overview/temperature-products/cryogenic-accessories/cryogenic-cable>.

Author contributions statement

All authors reviewed the manuscript.